

### **IN THE SPECIFICATION**

Please replace the paragraph beginning at page 15, line 18, with the following paragraph:

Still referring to Fig. 1, the slave station 200 preferably includes a processor 218, which can be selectively ~~stated~~ started and stopped under control of a switch 220. Advantageously, the processor 318 receives data from the storage device 216 and a second storage device 222, which stores data transmitted over the transceiver pair, line 128 and link 228. It will be noted that the data provided to the processor 218 from the storage device included both  $\lambda$  and  $I(t')$ , as discussed in greater detail below. The output of processor 218,  $\Delta T$ , i.e., the error between the master and slave clocks, is applied to the slave clock 218. It will also be noted that the transceiver pair 128, 228 advantageously form a secure communications channel.